IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

TRANSLATION CERTIFICATE
(not for PCT cases)

In re PATENT APPLICATION of
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Appln. No.10/

Attention: Application Division

Filed:March 25,2004

Title:TRAPEZOID SIGNAL GENERATING CIRCUIT

TRANSLATION STATEMENT
UNDER RULE 52(d)
FOR APPLICATION FILED IN FOREIGN LANGUAGE

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Sir:

The undersigned, of the below address, hereby states that he/she well knows both the English and Japanese languages, and that the attached is an accurate translation into the English language of the above-identified application, which was/is being filed in the aforesaid foreign language.

Signed this 23rd day of April, 2004.

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TRAPEZOID SIGNAL GENERATING CIRCUIT

CROSS REFERENCE TO RELATED APPLICATION

This application is based on and incorporates herein by reference Japanese Patent Application No. 2003-90967 filed on March 28, 2003.

FIELD OF THE INVENTION

The present invention relates to a trapezoid signal generating circuit, which generates a trapezoid signal by controlling a charging and discharging current of a capacitor.

BACKGROUND OF THE INVENTION

When a level of a rectangular signal changes, noises will arise due to harmonic components included in the sharp rising portions and the sharp falling portions of the rectangular signal. For instance, if the rectangular signal having the frequently changing levels is used in vehicle-mounted electronic devices, radio noises are generated. It is effective to use a trapezoid signal in place of the rectangular signal for reducing such noises.

JP-A-52-112263 discloses a waveform shaping circuit, which changes the inclination of one of the rising slope and the falling slope of a trapezoid signal in the middle of the slope. This circuit increases the inclination of the sharper one of the inclination-changed slopes to be sharper than the inclination of the other slope, which is not inclination-

changed. This circuit decreases the inclination of the less-sharper one of the inclination-changed slopes to be less-shaper than the inclination of the other slope, which is not inclination-changed. Specifically, this circuit has a capacitor, and changes a charging and discharging current of the capacitor in steps according to the terminal voltage of the capacitor.

Fig. 6 shows an example of a trapezoid signal generating circuit, and Fig. 7 shows the waveforms of operation signals of the trapezoid signal generating circuit 1. When an input signal Sin becomes a high level H, a switch 6 turns off via an inverter 5. A capacitor 2 is charged with an output current I1 of a constant current circuit 3. Thus, the output voltage Vo outputted via a buffer 7 linearly increases to a fixed level. When the input signal Sin becomes a low level L, the switch 6 turns on. The capacitor 2 is discharged with a current I1 which corresponds to the difference between the output currents of the constant current circuits 3 and 4. Thus, the output voltage Vo linearly decreases to zero.

In the voltage Vo (trapezoid signal) thus generated, the inclination stepwisely changes at the shoulder portions of its rising portion and falling portion (increase/decrease starting portion or increase/decrease ending portion). As a result, it is difficult to sufficiently reduce the harmonic components. Therefore, the above prior art proposes to reduce changes of the inclination at the shoulder portions by

changing the charging and discharging current in steps. In case of changing the charging and discharging current in steps in accordance with the terminal voltage of the capacitor 2, however, comparators in the number corresponding to the number of change steps are necessitated. The circuit size will be complicated more as the waveform is smoothed more.

SUMMARY OF THE INVENTION

Accordingly, it is an objective of the present invention to provide a trapezoid signal generating circuit, which generates a gradually changing trapezoid signal while minimizing a circuit size.

According to the present invention, a first and a second current output circuits for controlling a charging and a discharging of a capacitor are provided. A discharging current of the second current output circuit is set larger than a charging current of the first current output circuit. When a waveform control signal is at a first level, the capacitor is discharged with a difference current between the charging current and the discharging current. The rate of falling of a terminal voltage of the capacitor, that is, a trapezoid signal, is determined in accordance with the difference current. When the waveform control signal is at a second level, the discharging current is stopped. Thus, the capacitor is charged with the charging current of the first current output circuit. The rate of rising of the trapezoid

signal at this time is determined in accordance with the charging current.

The first and the second current output circuits are constructed to supply the charging current and the discharging current in accordance with command signals, respectively. A current control circuit is constructed to be able to continuously output the command signal like, for instance, a charging and discharging circuit described below. Thus, the charging current continuously increases after the time point when the waveform control signal changes from the first level to the second level, and continuously decreases after the time point when the trapezoid signal reaches a fixed reference level. In addition, both the charging current and the discharging current continuously increase after the time point when the waveform control signal changes from the second level to the first level, and continuously decreases after the time point when the trapezoid signal reaches the reference level.

The trapezoid signal results from an integration of the charging and discharging current. As a result, the inclination of the slope of the trapezoid signal at the shoulder portion (increase/decrease starting portion or increase/decrease ending portion) is changed very gradually by the above control, so that the harmonic components included in the trapezoid signal may be reduced. That is, a continuous current control is attained based on the command signal generated by the current control circuit, in stead of

a stepwise current control based on a terminal voltage of a capacitor. As a result, a plurality of comparators need not be used, and noise generation can be reduced while minimizing the circuit size as much as possible. Because the time point to change the charging and discharging current from an increase to a decrease is controlled based on a comparison of the trapezoid signal with the reference voltage, the terminal voltage of the capacitor after the rising and after the falling can be controlled.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an electric circuit diagram showing a trapezoid signal generating circuit according to the first embodiment of the present invention;

Fig. 2 is a waveform diagram showing signal waveforms appearing at various points in the first embodiment;

Fig. 3 is an electric circuit diagram showing a trapezoid signal generating circuit according to the second embodiment of the present invention;

Fig. 4 is a waveform diagram showing signal waveforms appearing at various points in the second embodiment;

Fig. 5 is a waveform diagram showing signal waveforms appearing at various points in the second embodiment in the case that an input signal is different;

Fig. 6 is an electric circuit diagram showing a trapezoid signal generating circuit according to a prior art; and

Fig. 7 is a waveform diagram showing signal waveforms appearing at various points in the prior art.

DETAILED DESCRIPTION OF THE INVENTION

(First embodiment)

A trapezoid signal generating circuit 11 shown in Fig. 1 is built in a control IC (semiconductor integrated circuit device) used in an ECU (electronic control unit) for controlling a chassis system of a vehicle such as doors, mirrors, seats, wipers, meters or an air-conditioner. This control IC also includes, in addition to this trapezoid signal generating circuit, digital circuits like a CPU or memories having various functions, and analog circuits having various functions.

The control IC has a function of receiving from a plurality of switches respective on/off conditions. Although not shown in the figure, one terminal of each switch is connected in common through a resistor, and the other terminal of each switch is grounded. A trapezoid signal generated by the trapezoid signal generating circuit 11 is applied periodically to the common terminal, so that the CPU responsively receives the voltage level of the one terminal of each switch through an input port. The trapezoid signal is applied periodically to the switches to reduce the current consumption and radio noises.

The trapezoid signal generating circuit 11 is constructed with a charging and discharging circuit 12 and a

current control circuit 13, and operable with a power supply voltage Vcc between power supply lines 14 and 15. The trapezoid signal is generated as a voltage Vo between both terminals of a capacitor 16. This voltage Vo is outputted through a buffer 17.

A current output circuit (first current output circuit) 18 is connected to the power supply line 14 and one terminal of the capacitor 16. A series circuit (second current output circuit) 21, which comprises a switch 19 constructed with a transistor and a current output circuit 20, is connected between the one terminal of the capacitor 16 and the power supply line 15, that is, between the terminals of the capacitor 16. The current output circuits 18 and 20 are for respectively supplying the charging current and the discharging current of the capacitor 16. The current output circuit 20 allows the current of two times (K = 2) of the current of the current output circuit 18.

The current output circuits 18 and 20 change the output currents in accordance with control signals applied thereto, respectively, while maintaining the relation of the current ratio of two. A V/I conversion circuit 22 receives a voltage (command signal) V1 outputted from the current control circuit 13, and applies control signals to the current output circuits 18 and 20 in correspondence with this voltage.

The switch 19 switches its on/off condition in response to an input signal (waveform control signal) Sin applied thereto through an inverter 23. Specifically, the switch 19

turns on in response to the L level (first level) of the input signal Sin, and turns off in response to the H level (second level) of the input signal Sin.

The current control circuit 13 is constructed with a charging and discharging circuit 24, a comparator 25 and an exclusive-OR gate 26. In the similar manner as the charging and discharging circuit 12, the charging and discharging circuit 24 is constructed with a capacitor (command signal capacitor) 27, a current output circuit 28 connected between the power supply line 14 and one terminal of the capacitor 27, a switch 20 and a current output circuit 30 connected in series between the terminals of the capacitor 27, and a V/I conversion circuit 31. A circuit portion of the charging and discharging circuit 24 other than the capacitor 27 operates as a charging and discharging current control circuit.

The comparator 25 is for comparing the voltage Vo with a reference voltage Va, which is one half of the power supply voltage Vcc. It produces a signal Sa, which becomes a L level and a H level when the voltage Vo becomes higher and lower than the reference voltage Va, respectively. The exclusive-OR gate 26 produces a signal Sb, which is an exclusive-OR logic of the input signal Sin and the signal Sa. The switch 29 turns off when the signal Sb becomes the L level, and turns on when the signal Sa becomes the H level.

Next, the operation of the trapezoid signal generating circuit 11 is described with reference to the input signal Sin, output signal Sa of the comparator 25, output signal Sb

of the gate 26, input voltage Vin, output voltage V1 of the current control circuit 13, current I2 flowing into the capacitor 27, current I1 flowing into the capacitor 16 and output voltage Vo of the trapezoid signal generating circuit 11 shown in Fig. 2. The input voltage Vin is a fixed level signal, and the input signal Sin is a periodic pulse signal having a fixed cycle period and a fixed H level time width. In Fig. 2, the waveforms are illustrated with shortened cycle period for convenience of illustration. The input signal Sin has in practice a cycle period of several tens of milliseconds and a H level time width of several hundreds of microseconds.

It is effective for reducing harmonic components at the rising portion and the falling portion of the voltage Vo, trapezoid signal, to gradually change the voltage changing rate (inclination) at the increase/decrease starting portions (A and C in Fig. 2) and at the increase/decrease ending portions (B and D in Fig. 2) of the voltage Vo. Therefore, the increase/decrease starting portion and the increase/decrease ending portion (shoulders) of the voltage Vo are changed continuously and smoothly in accordance with not a linear function (straight line) but with a quadratic function (curve line).

The terminal voltage Vo of the capacitor 16 results from an integration of the current I1 flowing into the capacitor 16. For this reason, the current I1 may be controlled as shown in Fig. 2, so that it increases in

accordance with a linear function from the time point when the input signal Sin changes from the L level to the H level, and thereafter decreases in accordance with a linear function. For this purpose, as shown in Fig. 2, the voltage V1 as the command signal is required to rise in accordance with a linear function from the time point of the change of the input signal Sin and thereafter fall in accordance with a linear function, if the voltage-current input and output characteristic of the V/I conversion circuit 22 and the current output circuits 18 and 20 is linear.

More specifically, since the voltage Vo is decreased to about 0 volt and lower than the reference voltage Va at time t1 in Fig. 2, the output signal Sa of the comparator 25 is at the H level. When the input signal Sin changes from the L level to the H level, the switch 19 turns off and the output signal Sb of the gate 26 becomes the L level to turn off the switch 29. As a result, a positive fixed current I2 flows from the current output circuit 28 into the capacitor 27, and the terminal voltage V1 of the capacitor 27 linearly rises from 0 volt. Thus, a linearly increasing current I1 flows from the current output circuit 18 into the capacitor 16. Accordingly, the voltage Vo rises with a gradually increasing inclination in accordance with the quadratic function.

When the voltage Vo exceeds the reference voltage Va at time point t2, the signal Sa changes from the H level to the L level and the signal Sb changes from the L level to the H level. As a result, the switch 29 turns on and a negative

fixed current I2 flows into the capacitor 27 so that the terminal voltage V1 of the capacitor 27 linearly falls. Thus, a linearly decreasing current I1 (> 0) flows from the current output circuit 18 into the capacitor 16. Accordingly, the voltage Vo rises with a gradually decreasing inclination in accordance with the quadratic function. The voltage Vo stops rising when the voltage V1 becomes 0 at time point t3.

The output current ratio between the current output circuit 20 and the current output circuit 18 and the output current ratio between the current output circuit 30 and the current output circuit 28 are set to two. In addition, the reference voltage Va is set to one half of Vcc. For this reason, the voltage Vo becomes generally equal to the power supply voltage Vcc. Further, the waveforms of the voltage Vo between the time points t1 and t2 and between the time points t2 and t3 becomes symmetric. This operation is similar to the operation when the voltage Vo falls in the period from a time point t4 to a time point t6.

The control IC periodically outputs the voltage Vo in the trapezoid waveform by using this trapezoid signal generating circuit 11, and is enabled to detect the on/off condition of each switch sequentially or concurrently in the period (from time point t3 to time point t4) in which the voltage Vo is generally equal to the power supply voltage Vcc.

As described above, the current output circuits 18 and 20 of the charging and discharging circuit 12 are constructed to allow the charging current and the discharging current in

accordance with the voltage V1 outputted from the current control circuit 13, respectively, in this embodiment. The current control circuit 13 is constructed to output the voltage V1, which increases and decreases in accordance with the linear function from the time point when the input signal Sin changes its level, by the charging and discharging circuit 24 of a single stage. As a result, the current I1 flowing into the capacitor 16 increases and decreases in accordance with the linear function, and the terminal voltage (trapezoid signal) Vo of the capacitor 16 rises and falls in accordance with the quadratic function. Thus, because the trapezoid signal changes its slopes gradually at it shoulders in waveform in particular, the harmonic components included in the trapezoid signal are reduced. Accordingly, the radio noises which will affect a radio receiver or other electronic devices mounted on a vehicle are reduced.

The trapezoid signal generating circuit 11 attains a continuous current control based on the voltage (command signal) V1 generated by the current control circuit 13. This is different from a stepwise current control, which may be attained based on the terminal voltage Vo of the capacitor 16. As a result, a smooth trapezoid signal can be generated without requiring a plurality of comparators. Thus, the circuit size is reduced and the cost of IC is reduced.

In addition, the current control circuit 13 compares the voltage Vo and the reference voltage Va by the use of a single comparator 25, and controls the magnitude of the

voltage V1 from an increase to a decrease when the voltage Vo reaches the reference voltage Va. For this reason, the voltage Vo can be controlled accurately after the rising and falling of the trapezoid signal.

(Second Embodiment)

Fig. 3 shows a trapezoid signal generating circuit, in which the same constructions as in Fig. 1 are represented with the same reference numerals. This trapezoid signal generating circuit 32 is different from the trapezoid signal generating circuit 11 shown in Fig. 1 in that a current control circuit 33 is constructed with cascade-connected two charging and discharging circuits 24 and 34.

The charging and discharging circuit 34 of the second stage is constructed with, in the similar manner as the charging and discharging circuit 24, a capacitor (command signal capacitor) 35, a current output circuit 36 connected between the power supply line 14 and one terminal of the capacitor 35, a switch 37 and a current output circuit 38 connected in series between the terminals of the capacitor 35, and a V/I conversion circuit 39. The switch 37 is constructed to be on/off-controlled by the signal Sb in the similar manner as the switch 29 is. The current output circuit 38 is constructed to output a two times current of the current output circuit 36. The charging and discharging circuit 34 other than the capacitor 35 corresponds to a charging and discharging circuit. This charging and discharging circuit 34 is constructed to receive the voltage

V1 from the charging and discharging circuit 24 and output a voltage (command signal) V2 to the charging and discharging circuit 12.

Fig. 4 shows the input signal Sin of a duty ratio of 50%, output signal Sa of the comparator 25, output signal Sb of the gate 26, input voltage Vin, output voltage V1 of the charging and discharging circuit 24 of the first stage, output voltage V2 of the charging and discharging circuit 34 (current control circuit 33), current I2 flowing into the capacitor 27, current I3 flowing into the capacitor 35, current I1 flowing into the capacitor 16 and output voltage Vo of the trapezoid signal generating circuit 11.

In this Fig. 4, the voltage V1, which the first-stage charging and discharging current circuit 24 in the current control circuit 33 outputs, is the same as the voltage V1 shown in Fig. 2. During the period from the time point t1 to the time point t2 in which the signal Sb is at the L level, a linearly increasing current I3 flows into the capacitor 35 from the current output circuit 36, and the voltage V2 rises in accordance with a quadratic function. Accordingly, a current I1 which increases in accordance with the quadratic function flows into the capacitor 16 from the current output circuit 18. Thus, the voltage Vo rises with a gradually increasing inclination in accordance with a cubic function.

During a time period from the time point t2 to time point t3 in which the signal Sb is at the H level, a linearly decreasing negative current I3 flows into the capacitor 35,

and the terminal voltage V2 of the capacitor 35 falls in accordance with a quadratic function. As a result, the current I1 (> 0) which decreases in accordance with the quadratic function flows into the capacitor 16 by the current output circuit 18 and 20. Thus, the voltage Vo rises with a gradually increasing inclination in accordance with the cubic function. When the voltage V2 falls to 0 at a time point t3, the voltage Vo stop rising. This operation is similar from a time point t4 to a time point t6, which corresponds to the falling portion of the voltage Vo.

In case that the duty ratio of the input signal Sin is only about several %, the signals at each circuit position results in a trapezoid signal Vo having a shortened time period t3 - t4 as shown in Fig. 5.

By constructing the current control circuit 33 with two charging and discharging circuits 24 and 33, the voltage V2 which is the command signal to the charging and discharging circuit 12 varies in accordance with the quadratic function, and the voltage Vo which is the trapezoid signal increases and decreases with the cubic function. As a result, the trapezoid signal is changed at a slower rate at its shoulders, and the harmonic components included in the trapezoid signal can be reduced more.

(Other Embodiments)

The present invention is not limited to the above embodiments, but may be modified as follows.

In the first embodiment, a certain offset voltage may

be provided so that the voltage V1 which is the command signal does not fall to 0 volt. With this offset voltage, an offset current continues to flow to discharge the capacitor 16 while the input signal Sin is at the L level, and the terminal voltage Vo of the capacitor 16 can be decreased to 0 volt without fail. In addition, the offset current continues to flow to charge the capacitor 16 while the input signal Sin is at the H level, and the terminal voltage Vo of the capacitor 16 can be increased to the power supply voltage Vcc without fail. Therefore, even when the capacitor 16 is repetitively charged and discharged, the capacitor 16 is prevented from producing an offset voltage between its terminals. A certain offset voltage is preferably provided similarly in the second embodiment, so that the voltage V2 does not fall to 0 volt.

The current control circuits 13 and 33 may be constructed with three or more cascade-connected charging and discharging circuits, or constructed with different circuits other than charging and discharging circuits.

The ratio of output currents of the current output circuit 20 and the current output circuit 18 is not limited to 2. Generally, the current output circuit 20 is only required to produce a current of K times (K > 1) of the current of the current output circuit 18. This relation is also applicable between the current output circuit 28 and the current output circuit 30 and between the current output circuit 36 and the current output circuit 38.

The reference voltage Va is not limited to one half of the power supply voltage Vcc.